REMARKS/ARGUMENTS

Claims 1-7, 9-16, and 23-27 are now pending in this application. Claims 1, 4, 7, and 23 are independent.

Claims 1, 4, 6, 7, 9-12, 14, 15, and 23-25 have been amended, claims 26 and 27 have been added, and claim 8 has been canceled by this amendment.

Amendment to the Specification

The Specification has been amended to incorporate the originally presented subject matter of claim 5, as is permitted under the Patent Rules. Thus, no new matter has been added to the Specification by this amendment.

Anticipation Rejection over Kim et al.

Withdrawal of the rejection of claims 1-4, 7-9, 12-13, 16, and 23-25 under 35 U.S.C. §102(b) as being anticipated by Kim et al. (US 5,441,904) is requested. Claim 8 has been canceled, thus rendering its rejection moot.

Applicant notes that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[2] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[3] To properly anticipate a claim, the reference must teach every element of the claim.[4] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[5] "The identical invention must be shown in as complete detail as is contained in the ...claim."[6] In determining anticipation, no claim limitation may be ignored.[7]

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[2] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[3] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[4] *See* MPEP § 2131.
[5] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[6] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[7] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

Background Discussion

By way of background, the present application, in various aspects, is directed to a method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, a method of forming a polycrystalline silicon structure in which crystal grain size varies as a function of depth, and a CMOS transistor in which the crystalline composition of the polysilicon is continuously varied as a function of distance measured from a surface of a dielectric film. The benefits of such a method and structure, as discussed in the Specification, include, but are not limited to, reduced polysilicon depletion, improved dopant activation, and a modulated resistance in the polysilicon gate electrode.

Discussion of Kim et al.

Kim et al. is directed to a method for forming a two-layered polysilicon gate electrode in a semiconductor device using discontinuous grain boundaries in two polysilicon layers having different grain sizes, with a silicide layer to prevent diffusion of fluorine gas through the grain boundaries. This structure prevents penetration of the fluorine gas into the gate oxide film.

Kim et al. does not disclose continuous variation of grain size by pressure and/or flow rate adjustment, and also does not disclose tailoring of polysilicon depletion next to the gate oxide by polysilicon grain size modulation.

In particular, Kim et al. does not disclose a method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, which includes, among other features, "...cooperatively selecting a second grain size in conjunction with the first size so as to maximize a dopant activation in a region near the gate dielectric; and contiguously with the crystals of the first size, depositing directly thereon additional polysilicon crystals of substantially the second size", as recited in independent claim 1, as amended.

Further, Kim et al. does not disclose method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, which includes, among other features, "...controlling a variation of at least one of temperature, pressure, and flow rate of a continuous flow of

silane...while depositing polysilicon therefrom as crystals of correspondingly controlled grain size; and forming a multi-region polycrystalline silicon deposition having regions with crystals of respectively different grain sizes by controlling said variation...", as recited in independent claim 4, as amended.

Still further, Kim et al. does not disclose a method of forming a polycrystalline silicon structure in which crystal grain size varies as a function of depth, which includes, among other features, "...controlling...the crystal grain size as a function of depth in the polysilicon structure; and forming a plurality of regions having respective different grain sizes", as recited in independent claim 7, as amended.

Finally, Kim et al. does not disclose a CMOS transistor, which includes, among other features, "...a gate conductor [which] includes a region of polycrystalline silicon...having a varying grain size as a function of a distance measured from a surface of the dielectric film", as recited in independent claim 23, as amended.

Accordingly, since the applied art does not disclose all the limitations recited in at least independent claims 1, 4, 7, and 23, particularly as amended, withdrawal of the anticipation rejections and allowance of these claims are respectfully requested.

Since dependent claims 2-6, 9-16, 24, and 25 variously and ultimately depend from allowable independent claims 1, 4, 7, and 23, these dependent claims are submitted as being allowable at least on that basis, without further recourse to the additional patentable features recited therein. Allowance of dependent claims 2-6, 9-16, 24, and 25 are requested.

Unpatentability Rejection over Kim et al. in View of Yew and Ozuturk

Withdrawal of the rejection of claims 5-6, 10-11, and 14-15 under 35 U.S.C. §103(a) as being unpatentable over Kim et al. in view of Yew et al. (US 6,150,251) and Ozuturk et al. (US 5,242,847) is requested.

Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references

themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the ***prior art reference must teach or suggest all the claim limitations.***[8] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[9]

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[10] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[11]

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[12] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[13] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[14]

Improper Motivation to Combine References

Applicants submit that, while Yew et al. may or may not teach "tailoring" the resistance of the top of the gate as asserted in the Official Action, the motivation to modify Kim et al. by the teachings of Yew et al. is submitted as being deficient.

The Examiner indicates that "it would have been obvious to...combine Yew with Kim, because the third layer will help with controlling the critical dimension of the gate during

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[8] *See* MPEP §2143.
[9] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[10] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[11] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[12] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[13] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).
[14] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

lithography." This motivation is submitted as not being on point, such that the Examiner's burden of establishing a *prima facie* case of unpatentability has not been met.

Controlling the critical dimension of the gate may be an important feature of Yew et al., but providing a solution to this technical problem is not a goal of Applicants' recited invention, nor is it even mentioned, as best as can be determined.

Two of Applicants' advantages, in furtherance of the general goals of reducing polysilicon depletion and modulating resistance in a polysilicon gate electrode, discussed at least at page 4 of the Specification, is to maximize dopant activation near the gate dielectric, and independently control the resistance of the polysilicon above a first region, i.e., in the upper small crystal size region located distal from the gate dielectric.

None of the applied art even addresses or recognizes the need for or the solution to these technical problems solved by Applicants' recited invention.

As the C.C.P.A. has held, "[w]hen a person, having the references before him and not cognizant of applicant's disclosure, would not be informed that a problem (solved by applicant's claimed invention) ever existed, such references (which failed to recognize the problem) could not have suggested its solution. The references were thus improperly combined since there is no suggestion in either of them that they can be combined to produce the result obtained by the claimed invention."[15] Thus, recognition of the problem to be solved is an important element in the determination of patentability.

Thus, Applicants submit that Yew et al. is not properly combinable with Kim et al., and thus also submit that a *prima facie* case of unpatentability has not been made.

Reference Combination does not Teach or Suggest all Limitations

Whether or not Yew et al. and Ozuturk et al. teach or suggest that for which they are offered by the Examiner, a proposition which Applicants do not agree for at least the reasons set

[15] *In re Shaffer*, 229 F. 2d 476, 108 U.S.P.Q. 326, 329 (C.C.P.A. 1956).

forth above, the applied art, alone or in combination, does not make up for the previously identified deficiencies of Kim et al., at least with respect to independent claims 4 and 7 from which dependent claims 6, 10-11, and 14-15 variously and ultimately depend, particularly with respect to the amendment of independent claims 4 and 7.

With respect to the Examiner's contention that selection of the recited layer rich in carbon atoms (dependent claim 14) and a layer of Si-Ge (dependent claim 15) is equivalent in functionality and is thus is a matter of design choice, Applicants respectfully traverse this assertion of equivalent layers in functionality, and the suggestion that an election of species may be necessary in this application.

In similar circumstances relating to claims to an apparatus, "[t]he BPAI held that appellant had simply made an obvious design choice. However, the different structures of appellant and of the reference achieve different purposes."[16] Further, "[t]o require an applicant to include in his specification evidence and arguments regarding whether particular subject matter was a matter of 'design choice' would be tantamount to requiring the applicant to divine, before an application is filed, rejections the PTO will proffer. ***A finding of 'obvious design choice' is precluded where claimed structure and the function it performs are different from those of the prior art***"[17] (emphasis added).

While Ozuturk et al. may disclose a layer of Si-Ge, the stated function of Si-Ge in this reference (see Abstract) is to allow shallow doped regions at the face of the semiconductor substrate without ion implantation.

In contrast, the function of the Si-Ge layer in Applicants' recited invention (claim 15) is to further facilitate a higher level of dopant activation, or to provide a break in the dopant distribution, in order, for example, to allow for improved gate performance. See Specification at least at page 6.

Similarly, the carbon rich layer performs a different function than the Si-Ge layer in the

[16] *In re Gal*, 25 USPQ 2d 1076, 1078 (Fed. Cir. 1992).
[17] *In re Chu*, 36 USPQ 2d 1089, 1095 (Fed. Cir. 1995).

applied art. Therefore, since the functions performed by the claimed limitation are different from the applied art, withdrawal of the assertion of "design choice" is respectfully requested.

In the event that the Examiner still maintains that an election of species between a Si-Ge or carbon rich layer is required, then Applicants provisionally elect Si-Ge, with traverse.

Since the applied art, taken alone or in combination, does not teach or suggest all the claimed limitations, reconsideration and allowance of claims 6, 10-11, and 14-15 are respectfully requested.

35 U.S.C. §112, ¶1 Written Description Rejection

Withdrawal of the rejection of claim 5 under 35 U.S.C. §112, first paragraph, as lacking written description support, is requested.

The subject matter of originally presented claims 4 and 5 has been incorporated into the Specification, as permitted by the MPEP, and as discussed above.

Therefore, since the subject matter of claim 5 is now properly found in the Specification, as amended, withdrawal of the §112, ¶1 rejection for lack of written description support is requested.

Conclusion

In view of the above, each of the presently pending claims 1-7, 9-16, and 23-27 in this divisional application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner believes that an interview would serve to resolve any remaining issues in this application or would otherwise expedite passage of the application to issue, the undersigned attorney is available at the telephone number indicated below.

Application No.: 10/616,962

Docket No.: 21806-00113-US1

Although no fees are believed to be due, for any fees that may be due, please charge IBM Deposit Account No. 09-0456, under Order No. BUR-2000-0039-US2 (CBLH 21806-00113-US1) from which the undersigned is authorized to draw.

Respectfully submitted,

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